## CLAIMS

1. A method of forming a vertical double gate semiconductor device comprising:

providing a semiconductor substrate;

providing a first insulating layer over the semiconductor substrate;

providing a first semiconductor layer over the first insulating layer;

removing portions of the first semiconductor layer to form a semiconductor structure having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall;

forming a first current electrode region and a second current electrode region in the semiconductor substrate;

forming a second insulating layer adjacent the first sidewall and the second sidewall;

forming a conductive layer over the semiconductor structure and the second insulating layer; and

removing a portion of the conductive layer to form a first electrode region and a second electrode region, wherein:

the first electrode region is adjacent the first sidewall of the semiconductor structure;

the second electrode region is adjacent the second sidewall of the semiconductor structure; and

the first electrode region and the second electrode region are physically isolated from each other.

2. The method of claim 1 wherein the semiconductor structure is a channel region of the vertical double gate semiconductor device.

3. The method of claim 1 wherein removing the portions of the conductive layer comprises anisotropically etching the conductive layer.

4. The method of claim 1 wherein removing the portions of the conductive layer comprises planarizing the conductive layer.

5. The method of claim 1 wherein forming the conductive layer further comprises:

forming a second semiconductor layer; and

doping the second semiconductor layer in a first area adjacent the semiconductor structure with a first species.

6. The method of claim 5, further comprising doping the second semiconductor layer in a second area adjacent the semiconductor structure with a second species, wherein the second species is different than the first species and the second area is different than the first area.

7. The method of claim 6, wherein doping the second semiconductor layer is performed by ion implantation at an angle relative to a top surface of the semiconductor substrate.

8. The method of claim 6, further comprising annealing the first electrode region and the second electrode region after doping the second semiconductor layer.

9. The method of claim 6, wherein removing a portion of the conductive layer is performed after doping the second semiconductor layer in a first area adjacent the semiconductor structure with a first species.

10. The method of claim 6, wherein the first area is part of the first electrode region and the second area is part of the second electrode region.

11. The method of claim 1, further comprising forming metal over the first electrode region and the second electrode region.

12. The method of claim 11, wherein forming the metal comprises:

forming a silicon layer over the first electrode region, the second electrode region, and the semiconductor structure;

forming a first metal layer over the silicon layer; and

heating the semiconductor substrate so that the silicon layer and the first metal layer form a silicide.

13. The method of claim 12, further comprising: removing a portion of the metal to form a first contact for the first electrode region and a second contact for the second electrode region, wherein the first contact and the second contact are electrically isolated from each other.

14. The method of claim 13, wherein removing a portion of the metal comprises planarizing the metal.

15. The method of claim 11, further comprising annealing the first electrode region and the second electrode region before forming the metal .

16. The method of claim 11, wherein the metal is a stack of metal layers.

17. A method of forming a vertical double gate semiconductor device comprising:

providing a semiconductor substrate;

forming a first insulating layer over the semiconductor substrate;

forming a first semiconductor layer on the first insulating layer;

etching portions of the first semiconductor layer to form a semiconductor structure having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall in a first direction;

forming a source region and a drain region in the semiconductor substrate in a second direction, wherein the first direction is substantially perpendicular the second direction;

forming a second insulating layer on the first sidewall and the second sidewall;

forming a second semiconductor layer over the semiconductor structure and the second insulating layer, wherein the second semiconductor layer comprises:

a first semiconductor portion which is adjacent the first sidewall;

a second semiconductor portion which is over the semiconductor structure; and

a third semiconductor portion which is adjacent the second sidewall;

doping the first semiconductor portion and the third semiconductor portion; and

removing the second semiconductor portion.

18. The method of claim 17, wherein the second insulating layer is deposited conformally.

19. The method of claim 17 further comprising annealing the second semiconductor layer.

20. The method of claim 19 wherein annealing is performed after removing the second semiconductor portion.

21. The method of claim 17 wherein removing the second portion is performed by a method selected from the group of anisotropic etching, planarization and etch back.

22. The method of claim 17 wherein doping the first semiconductor portion and the third semiconductor portion further comprises doping the first semiconductor portion with a first species and doping the third semiconductor portion with a second species, wherein the first species and the second species are different in conductivity.

23. The method of claim 17, wherein doping the first semiconductor portion and the third semiconductor portion is performed by ion implanting species at an angle relative to a top surface of the semiconductor substrate.

24. The method of claim 17, wherein doping the first semiconductor portion and the third semiconductor portion further includes forming a patterned layer over the semiconductor substrate.

25. The method of claim 17, wherein etching portions of the first semiconductor layer to form the semiconductor structure further comprises:

forming a third insulating layer over the first semiconductor layer;

forming a nitride layer over the third insulating layer;

patterning the nitride layer and the third insulating layer; and

etching the first semiconductor layer using the nitride layer and the third insulating layer as a mask.

26. A vertical double gate semiconductor device comprising:

a semiconductor substrate;

a first insulating layer over the semiconductor substrate;

a semiconductor structure over the first insulating layer having a first current electrode region, a second current electrode region, a first sidewall and a second sidewall, wherein:

the first current electrode region and the second current electrode region are separated by a channel region in a first direction; and

the first sidewall and the second sidewall are opposite each other in a second direction, wherein the first direction is substantially perpendicular to the second direction;

a first control electrode region over the first sidewall; and

a second control electrode region over the second sidewall, wherein the first control electrode region and second control electrode region are not contiguous portions of a same material.

27. The vertical double gate semiconductor device of claim 26 wherein the first control electrode region and the second control electrode region are doped.

28. The vertical double gate semiconductor device of claim 26 wherein the first control electrode region is doped with a different species than the second control electrode region.

29. The vertical double gate semiconductor device of claim 26 wherein the first control electrode region is doped n-type and the second control electrode region is doped p-type.

30. The vertical double gate semiconductor device of claim 26 wherein a first contact is formed over the first control electrode region and a second contact is formed over the second control electrode region, wherein the first contact and the second contact are electrically isolated from each other.

31. The vertical double gate semiconductor device of claim 26 wherein a metallic layer is formed over the first control electrode region, the second control electrode region and the channel region.

32. The vertical double gate semiconductor device of claim 31 wherein the metallic layer comprises a metal nitride layer or a metal silicon nitride layer.

33. The vertical double gate semiconductor device of claim 26 wherein the semiconductor substrate and the semiconductor structure comprise silicon.